# MIPS64™ 5K™ LV (5Kc, TSMC 5KcH01X01) Specification Update

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# 1 Preface

This document communicates updates to the specifications of the family of MIPS32™ 4K™ and MIPS64™ 5K™ Processor Lead Vehicles contained in the document *MIPS 4K/5K™ Lead Vehicle Datasheet,* Ref [1].

There are variations in the characteristics of the Lead Vehicles. These are due to the variations in the type, revision, and configuration of the Lead Vehicle, and they are dependent on the vendor, the process technology, and the production series. Through the on-going validation and characterization of the Lead Vehicles, MIPS identifies updates and additions to the information in the documentation for the Lead Vehicles. The Specification Updates in this document are specific to the

- *MIPS64 5Kc Processor Lead Vehicle with manufacturing ID TSMC 5KcH01X01*.

The Specification Updates can be classified as deviations from the generic specifications, additional information, or defects.

The document is primarily intended for hardware system developers building boards equipped with MIPS32 4K or MIPS64 5K Processor Lead Vehicles.

The document presents additional information and detailed descriptions of deviations from the specifications in the datasheet. There are sections for updates to the chip pin description, AC & DC specifications, power supply, operating frequency, and other specification updates.

All 4K/5K LV's provides the ability for software to configure certain aspects of the physical hardware configuration, most notably the cache configuration can be "downgraded" under software control to experiment with the performance effects. This configuration ability is described in Ref [3].

Defects are listed in overview form in the errata information section. A detailed description of the defects are given in section 3. This includes description of the problem, the implication on the system, a suggested work around, and status. The status of an errata will be described by one of the following codes:

**Table 1 Status Codes Used In Summary Tables**

| Code | Description |
|---|---|
| Open | This issue is under investigation. |
| Fix | This issue is intended to be fixed in a future version of the component. |
| Fixed | This issue has been fixed in a previous version. |
| NoFix | There are no plans to fix this issue. |
| Doc | The appropriate documents will be updated in the future. |

## 1.1 Emphasis of Range Violations and Document Modifications

Throughout the document a shaded field in a table is used to emphasize that this value is deviating from, or violating, the range specified in the datasheet.



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# 2 Specification Updates to TSMC 5KcH01X01

In this section specific information on this particular Lead Vehicle is provided. The information is structured as a set of sub-sections containing specifications that must be present for each Lead Vehicle. These sub-sections are a supplement to the datasheet and consist of

- Basic Information
- Errata Information
- Supply Voltages and Environmental Conditions
- Test-related Pin-out
- DC Specifications
- AC Specifications
- PLL Connections and Loop Filter

The remaining sections contains Specification Updates that are unique for this Lead Vehicle and thus not covered elsewhere.

## 2.1 Basic Information

The basic information for the Lead Vehicle is summarized in Table 2.

**Table 2 Lead Vehicle Information**

| Parameter | Value |
|---|---|
| Vendor | TSMC |
| Type | 5Kc core |
| Part ID | 5KcH01X01 |
| Data Cache | 4-way, 16kByte sets, 64kByte total, no Parity |
| Instruction Cache | 4-way, 16kByte sets, 64kByte total, no Parity |
| MMU | TLB with 32 dual entries |
| EJTAG Support | Version 2.5<br>4 I breaks, 2 D breaks, TAP module |
| RTL Version | 2.3.0 |
| Static Input Signals to Core:<br><br>EJ_ManufID[10:0]<br>EJ_PartNumber[15:0]<br><br>EJ_Version[3:0] | <br><br>0x127<br>0x0310<br><br>0x0 |
| CP0 PRID Value | 0x018108 |



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## 2.2 Errata Information

Table 3 contains an overview of the present errata information on this LV implementation of the MIPS 5Kc. The listed errata information only concerns the LV implementation and not the MIPS 5Kc itself. For errata information on the latter see Ref [2] Section 3 contains a detailed description of the LV errata.

**Table 3 Errata information**

| Errata# | Description |
|---|---|
| L1 | SysAD64 mode non functional |

## 2.3 Supply Voltages and Environmental Conditions

The Lead Vehicle's three power supply voltages, the I/O power supply, the core power supply, and the PLL power supply (quiet Vss, Vdd) are listed in Table 4 together with the operating ambient temperature.

**Table 4 Supply Voltages and Operating Ambient Temperature**

| Parameter | Value | Tolerance |
|---|---|---|
| VDD (I/O buffers) | 3.3 V | 10 % |
| CVDD (Core supply) | 1.8 V | 10 % |
| VDDA (PLL supply) | 1.8V | 10 % |
| Operating ambient temperature | 0 $^{o}$C to +70 $^{o}$C | - |

When powering on the power supplies, it is recommended to first power up the I/O VDD supply followed by the CVDD and VDDA supplies. The recommended power-down order of the supplies is the reverse of the power-up order; first power down the CVDD and VDDA supplies, then power down the I/O VDD supply.

## 2.4 Test-related Pin-out

The following table lists deviations and additions to the functional pin descriptions given in the datasheet. Table 5 shows the format of the implementor test pins. The test pins are only for internal undocumented use. The input pins should be left de-asserted.

**Table 5 Test Pin Description**

| Test mode pins (implementor use only) | | | |
|---|---|---|---|
| **Pin name** | **Type** | **Control Pin** | **Description** |
| TIN[0] | I | | Memory BIST enable |
| TIN[1] | I | | MIPS test structure clock |
| TIN[2] | I | | MIPS test structure data |
| TIN[3] | I | | MIPS test structure enable |
| TIN_N[0] | I | | Tri-state test signal, when asserted forces all tri-state buffers to be tri-stated |
| TIN_N[1] | I | | MIPS test structure reset |
| TIN_N[2] | I | | Disable VDDOK (disables internal VDDOK generation) |
| TIN_N[3] | I | | External PLL reset (PLL reset pin, active low) |



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**Table 5 Test Pin Description**

| Test mode pins (implementor use only) | | | |
|---|---|---|---|
| **Pin name** | **Type** | **Control Pin** | **Description** |
| TOUT[0] | O | | MIPS test structure output |
| TOUT[1] | O | | Memory BIST done |
| TOUT[2] | O | | Memory BIST fail |
| TOUT[3] | O | | PLL output clock |

## 2.5 DC Specifications

The I/O cells on this Lead Vehicle are from the Artisan TSMC I/O library TPZ973G (release 200c). There are several types of input-only, output-only, and input/output buffers used in this Lead Vehicle. DC operating conditions are described in Table 6. Input and output voltage levels are shown in Table 7.

**Table 6 Recommended Operating Condition**

| Parameter | Description | Min | Nom | Max |
|---|---|---|---|---|
| VDD | I/O buffer supply voltage | 3.0 V | 3.3 V | 3.6 V |
| CVDD | Core supply voltage | 1.62 V | 1.8 V | 1.98 V |
| VDDA | Analog supply voltage | 1.62 V | 1.8 V | 1.98 V |
| $V_I$ | Input voltage | -0.3 V | | 5.5 V |
| $V_O$ | Output voltage | 0 V | | VDD |
| $V_{IH}$ | High-level input voltage | 2.0 V | | 5.5 V |
| $V_{IL}$ | Low-level input voltage | -0.3 V | | 0.8 V |

**Table 7 Electrical Characteristics**

| Parameter | Condition | Min | Max |
|---|---|---|---|
| $V_{OH}$ | $I_O$ = -16 mA, VDD = min | 2.4 V | |
| $V_{OL}$ | $I_O$ = 16 mA, VDD = min | | 0.4 V |
| $I_{IH}$ | $V_I$ = 3.3 V, VDD = max | | +/- 1 µA |
| $I_{IL}$ | $V_I$ = 0 V, VDD = max | | +/- 1 µA |
| $I_{OZ}$ | VDD = max | | +/- 1 µA |

The input receivers all use the same CMOS input-only, non-inverting pad, PDIDGZ. The output pads are all 3.3V CMOS outputs. Several types of output pads are used as described in Table 8. For the output drivers, the rated AC drive currents, $I_{OL}$ and $I_{OH}$, are included as well.

**Table 8 Driver Characteristics**

| Driver | Description | I/O | $I_{OL}$ @ 0.4 V | $I_{OH}$ @ 2.4 V |
|---|---|---|---|---|
| PDIDGZ | CMOS input-only pad | I | N/A | N/A |
| PDO04CDG | CMOS output-only pad | O | 4.5 mA | 6.2 mA |



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**Table 8 Driver Characteristics**

| Driver | Description | I/O | $I_{OL}$ @ 0.4 V | $I_{OH}$ @ 2.4 V |
|---|---|---|---|---|
| PDO08CDG | CMOS output-only pad | O | 8.9 mA | 12.4 mA |
| PRO08CDG | CMOS output-only pad with limited slew | O | 8.9 mA | 12.4 mA |
| PDT16DGZ | CMOS tristate output-only pad | O | 17.9 mA | 24.7 mA |
| PDB16DGZ | CMOS input/output pad | I/O | 17.9 mA | 24.7 mA |

## 2.6 AC Specifications

This section shows any deviations of the AC specifications from the corresponding descriptions in the Datasheet. First, an overview of the clock AC specifications is provided. Then, tables for the AC requirements of the pins are presented.

### 2.6.1 Clock Signals

Table 9 shows the frequency and duty cycle ranges for all the input clock pins in the Lead Vehicle. The duty cycle is here specified as the percentage of the cycle where the phase is high.

**Table 9 Clocking Frequency and Duty Cycle Range**

| Pin, Mode | Min | Max |
|---|---|---|
| Core clock frequency range | 0 MHz | 200 MHz |
| | | |
| GCLK frequency range, core bond-out (PLL disabled) | 0 MHz | 83 MHz |
| GCLK duty cycle, core bond-out (PLL disabled) | 40 | 60 |
| | | |
| ETCK frequency range | 0 MHz | 125 MHz |
| ETCK duty cycle | 45 | 55 |

### 2.6.2 Other functional pins

The following three tables lists the AC/DC pin specifications.

**Table 10 AC/DC Pin Specifications For Shared Function Pins**

| Pin name | Type | Buffer Type | External load [pF] | Reference Clock | Clk2out min [ns] | Clk2out max [ns] | Input setup [ns] | Input hold [ns] |
|---|---|---|---|---|---|---|---|---|
| GCLK | I | PDIDGZ | | - | | | | |
| GCLKB | O | PDO08CDG | 25 | CoreCLK | 0.2 | 1.5 | | |
| GRST2_N | I | PDIDGZ | | DC | | | | |
| GBYPASS | I | PDIDGZ | | DC | | | | |
| GMULT[1:0] | I | PDIDGZ | | DC | | | | |



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**Table 10 AC/DC Pin Specifications For Shared Function Pins**

| Pin name | Type | Buffer Type | External load [pF] | Reference Clock | Clk2out min [ns] | Clk2out max [ns] | Input setup [ns] | Input hold [ns] |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | |
| CBIGEN | I | PDIDGZ | | DC | | | | |
| CTIMER5 | I | PDIDGZ | | DC | | | | |
| CSYSAD | I | PDIDGZ | | DC | | | | |
| CPIPEWR | I | PDIDGZ | | DC | | | | |
| C4WBLK | I | PDIDGZ | | DC | | | | |
| | | | | | | | | |
| ETCK | I | PDIDGZ | | - | | | | |
| ETMS | I | PDIDGZ | | DC | | | | |
| ETDI | I | PDIDGZ | | ETCK | | | 4 | 1 |
| ETDO | O (3S) | PDT16DGZ | 50 | ETCK[a] | 2 | 8.4 | | |
| ETRST_N | I | PDIDGZ | | DC | | | | |
| EDINT | I | PDIDGZ | | ASYNC | | | | |
| ERES[1:0] | O | PRO08CDG | 50 | | | | | |
| | | | | | | | | |
| TR_Probe_n | I | PDIDGZ | | DC | | | | |
| TR_TrigIn | I | PDIDGZ | | ASYNC | | | | |
| TR_TrigOut | O | PRO08CDG | | ASYNC | | | | |
| TR_Clk | O | PRO08CDG | | | | | | |
| TR_Data[7:0] | O | PRO08CDG | | TR_Clk | | | | |
| TR_DM | O | PRO08CDG | | ASYNC | | | | |
| | | | | | | | | |
| TSE | I | PDIDGZ | | DC | | | | |
| TSM | I | PDIDGZ | | DC | | | | |
| TSI | I | PDIDGZ | | DC | | | | |
| TSO | O | PDO08CDG | 25 | | | | | |
| TIN[3:0] | I | PDIDGZ | | DC | | | | |
| TIN_N[3:0] | I | PDIDGZ | | DC | | | | |
| TOUT[3:0] | O | PDO08CDG | | | | | | |
| | | | | | | | | |
| MBUS | I | PDIDGZ | | DC | | | | |



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**Table 10 AC/DC Pin Specifications For Shared Function Pins**

| Pin name | Type | Buffer Type | External load [pF] | Reference Clock | Clk2out min [ns] | Clk2out max [ns] | Input setup [ns] | Input hold [ns] |
|---|---|---|---|---|---|---|---|---|
| MINP[2:0] | I | PDIDGZ | | DC | | | | |
| MINP_N[2:0] | I | PDIDGZ | | DC | | | | |

a. The ETDO output timing is specified relative to the negative edge of ETCK.

**Table 11 AC/DC pin specs for core bond-out mode**

| Pin name | Type | Buffer Type | External load [pF] | Reference Clock | Clk2out min [ns] | Clk2out max [ns] | Input setup [ns] | Input hold [ns] |
|---|---|---|---|---|---|---|---|---|
| EB_A[35:3] | O | PDB16DGZ | 25 | GCLK | 3 | 10 | | |
| EB_WData[63:28] | O | PDO08CDG | 25 | GCLK | 3 | 10.6 | | |
| EB_WData[27:0] | O | PDB16DGZ | 25 | GCLK | 3 | 10.6 | | |
| EB_RData[63:0] | I | PDIDGZ | | GCLK | | | 6 | 0 |
| EB_BE[7:0] | O | PDB16DGZ | 25 | GCLK | 3 | 10 | | |
| EB_AValid | O | PDB16DGZ | 25 | GCLK | 3 | 10 | | |
| EB_Write | O | PDB16DGZ | 25 | GCLK | 3 | 10 | | |
| EB_Instr | O | PDB16DGZ | 25 | GCLK | 3 | 10 | | |
| EB_Burst | O | PDB16DGZ | 25 | GCLK | 3 | 10 | | |
| EB_BFirst | O | PDB16DGZ | 25 | GCLK | 3 | 10 | | |
| EB_BLast | O | PDB16DGZ | 25 | GCLK | 3 | 10 | | |
| EB_BLen[1:0] | O | PDB16DGZ | 25 | GCLK | 3 | 10 | | |
| EB_ARdy | I | PDIDGZ | | GCLK | | | 6 | 0 |
| EB_RdVal | I | PDIDGZ | | GCLK | | | 6 | 0 |
| EB_WDRdy | I | PDIDGZ | | GCLK | | | 6 | 0 |
| EB_RBErr | I | PDIDGZ | | GCLK | | | 6 | 0 |
| EB_WBErr | I | PDIDGZ | | GCLK | | | 6 | 0 |
| EB_WWBE | O | PDB16DGZ | 25 | GCLK | 3 | 10 | | |
| EB_EWBE | I | PDIDGZ | | GCLK | | | 6 | 0 |
| EB_SBlock | I | PDIDGZ | | GCLK | | | 6 | 0 |
| | | | | | | | | |
| SI_Int[5:0] | I | PDIDGZ | | GCLK | | | 6 | 0 |
| SI_NMI | I | PDIDGZ | | GCLK | | | 6 | 0 |
| SI_ColdReset | I | PDIDGZ | | GCLK | | | 6 | 0 |



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**Table 11 AC/DC pin specs for core bond-out mode (Continued)**

| Pin name | Type | Buffer Type | External load [pF] | Reference Clock | Clk2out min [ns] | Clk2out max [ns] | Input setup [ns] | Input hold [ns] |
|---|---|---|---|---|---|---|---|---|
| SI_Reset | I | PDIDGZ | | GCLK | | | 6 | 0 |
| SI_MergeMode[1] | I | PDIDGZ | | GCLK | | | 6 | 0 |
| SI_SimpleBE[0] | I | PDIDGZ | | GCLK | | | 6 | 0 |
| SI_RP | O | PDO08CDG | 25 | GCLK | 3 | 10.5 | | |
| SI_Sleep | O | PDB16DGZ | 25 | GCLK | 3 | 10 | | |
| SI_TimerInt | O | PRO08CDG | 25 | GCLK | 3 | 10.1 | | |
| SI_ERL | O | PRO08CDG | 25 | GCLK | 3 | 10 | | |
| SI_EXL | O | PDO08CDG | 25 | GCLK | 3 | 10 | | |
| | | | | | | | | |
| EJ_PerRst | O | PDO08CDG | 25 | GCLK | 3 | 10.4 | | |
| EJ_PrRst | O | PDO08CDG | 25 | GCLK | 3 | 10.3 | | |
| EJ_SRstE | O | PDO08CDG | 25 | GCLK | 3 | 10 | | |
| EJ_DebugM | O | PDO08CDG | 25 | GCLK | 3 | 10.1 | | |
| | | | | | | | | |
| PM_DCacheHit | O | PDO08CDG | 25 | GCLK | 3 | 10 | | |
| PM_DCacheMiss | O | PDO08CDG | 25 | GCLK | 3 | 10 | | |
| PM_ICacheHit | O | PDO08CDG | 25 | GCLK | 3 | 10 | | |
| PM_ICacheMiss | O | PDO08CDG | 25 | GCLK | 3 | 10 | | |
| PM_InstnComplete | O | PDO08CDG | 25 | GCLK | 3 | 10 | | |
| PM_ITLBHit | O | PDO08CDG | 25 | GCLK | 3 | 10 | | |
| PM_ITLBMiss | O | PDO08CDG | 25 | GCLK | 3 | 10 | | |
| PM_JTLBHit | O | PDO08CDG | 25 | GCLK | 3 | 10 | | |
| PM_JTLBMiss | O | PDO08CDG | 25 | GCLK | 3 | 10.2 | | |
| PM_WTBMerge | O | PDO08CDG | 25 | GCLK | 3 | 10 | | |
| PM_WTBNoMerge | O | PDO08CDG | 25 | GCLK | 3 | 10 | | |
| PM_DTLBHit | O | PDO08CDG | 25 | GCLK | 3 | 10.4 | | |
| PM_DTLBMiss | O | PDO08CDG | 25 | GCLK | 3 | 11.5 | | |



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## 2.7 PLL Connections and Loop Filter

Table 12 shows the pin-out for the 6 analog connections to the PLL (quiet supplies, optional loop filter etc.).

**Table 12 PLL Pin-Out**

| Pin Name | Ball No. | Buffer type | Package Connection |
|---|---|---|---|
| VDDA | B12 | supply | Clean analog supply |
| VSSA | A13 | supply | Clean analog supply |
| PLL_NC[2] | B13 | PDIDGZ | Connect to logic 0 (VSSA or VSS) |
| PLL_NC[1] | D13 | PDIDGZ | Connect to logic 0 (VSSA or VSS) |
| PLL_NC[0] | C13 | PDO04CDG | Leave unconnected |
| LF | C14 | PDO04CDG | Leave unconnected |

This Lead Vehicle uses an internal loop filter.



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# 3 LV Errata

***L1. SysAD64 mode non functional***

Problem:

SysAD64 mode is non functional.

Implication:

The device is only functional in core bond-out mode.

Work around:

None.

Status:

Fix (if a new version is made).



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# 4 References

[1] MIPS 4K/5K™ Lead Vehicle Datasheet
Document no: MD00001
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[2] MIPS64 5K™ Processor Core Family RTL Errata Sheet
Document no: MD00031
MIPS Technologies, Inc.

[3] MIPS 4K™/5K™ Cache Configuration Application Note
Document no: MD00213
MIPS Technologies, Inc.



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# 5 Revision history

| Rev. Number | Date | Comments |
|---|---|---|
| 01.00 | October 30, 2001 | First official release. |
| 01.01 | December 6, 2001 | Updated with STA data after tape-out. |
| 01.02 | January 24, 2002 | Minor changes made before use at chiptester. |
| 01.03 | June 4, 2002 | I/O macro names corrected.<br>Software configuration chapter removed and replaced with reference.to MD00213.<br>Updates from the characterization process added.<br>SysAD specific information changed to conditional text. |



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